REMARKS

Claims 1-34 and 58-71 are pending in the present application. Reconsideration and allowance of pending claims 1-34 and 58-71 in view of the following remarks are requested.

In the Office Action dated November 3, 2004, the Examiner has ***finally rejected*** claims 1-34 and 58-71 pending in the present application on the basis of a new ground of rejection. Applicant respectfully requests reconsideration and withdrawal of the finality of the rejection of the Office Action dated November 3, 2004. A good and sufficient reason why the present response is necessary and was not earlier presented is that a new ground of rejection (see page 6 of the Office Action, paragraph 7) has been relied upon in the present final rejection (37 CFR §1.116(c)). The new ground of rejection was not relied upon prior to the instant final rejection. Applicant believes that it would be manifestly unfair for the Patent Office not to consider Applicant's arguments which are necessitated due to the Examiner's new ground of rejection. As such, a good and sufficient reason exists, as required by 37 CFR §1.116(c), for considering Applicant's present response and withdrawing the finality of the present Office Action.

A. Objection to the Drawings

The PTO Draftsperson has objected to the drawings for reasons noted on the Notice of Draftsperson's Patent Drawing Review (PTO-948), dated May 27, 2003. Applicant has amended Figures 5 and 8 by adjusting the top and left margins to comply with 37 CFR § 1.84(g). Applicant has also amended Figures 1-4 and 8 by replacing solid

black shading with hatching to comply with 37 CFR § 1.84(m). Applicant notes that the solid black areas that remain in Figure 8 are used to designate contacts, which are commonly represented in the art as black squares. Furthermore, in Figure 8 of the parent of the present application, which has issued as U.S. patent number 6,762,441, solid black squares are also used to designate contacts. Applicant has enclosed herein six (6) replacement sheets including Figures 1-4, 5, and 8.

B. Rejection of Claims 1-34 and 58-71 under 35 USC §112, first paragraph

The Examiner has rejected claims 1-34 and 58-71 under 35 USC §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, the Examiner has stated that "Applicant has not shown, nor is it known to the art, how to tie the 'Pinned Transfer Gate' to the potential of the substrate." Page 3 of the Office Action dated November 3, 2004. Applicant respectfully disagrees with the Examiner for the following reasons.

As an example, in U.S. patent number 5,077,592 to James R. Janesick ("Janesick") which is cited by the PTO in the prosecution file of the parent application as well as the present application, Janesick discloses an open pinned-phase pixel having an open-phase region including n-channel 10 having a shallow implant of p-type doping, which pins the surface potential to zero volts at the interface between thin oxide film 18 and n-channel 10 in the open phase region. See, for example, column 4, lines 39-49 and Figure 1 of

Janesick. Thus, Janesick discloses how to "pin" the surface potential of an open phase region of an open pinned-phase pixel to zero volts by forming a shallow implant of p-type doping in an n-channel, which connects the surface potential to the voltage of a substrate and acts as a virtual gate. Thus, Applicant respectfully submits that the teachings of Janesick can be used by one of ordinary skill in the art to manufacture the pinned transfer gate disclosed in the present application.

By way of further example, in U.S. patent number 4,994,875 to Jaroslay Hynecek ("Hynecek") which is also cited by the PTO in the prosecution file of the parent application as well as the present application, Hynecek discloses a charge transfer device including P-type inversion layer 14 and P+ channel-stop region 18, where P-type inversion layer 14 is electrically connected to P+ channel-stop region 18 and P+ channel-stop region 18 is electrically connected to substrate 11. See, for example, column 2, lines 57-68, column 3, lines 1-5 and lines 53-61, and Figure 1 of Hynecek. In Hynecek, P-type inversion layer 14 is connected to a voltage of substrate 11 by P+ channel-stop region 18. In Hynecek, P-type inversion layer 14 functions as a "virtual electrode" of a "virtual gate" to prevent electrons from transferring until a conductive electrode reaches a critical voltage. Thus, Applicant respectfully submits that the teachings of Hynecek can also be used by one of ordinary skill I the art to manufacture the pinned transfer gate disclosed in the present application. Accordingly, Applicant respectfully submits that the requirements of 35 USC §112, first paragraph, have been met.

C. **Rejection of Claims 1 and 5-8 under 35 USC §102(e)**

The Examiner has rejected claims 1 and 5-8 under 35 USC §102(e) as being anticipated by U.S. patent number 6,603,144 B2 to Shiro Tsunai ("Tsunai"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claim 1, is patentably distinguishable over Tsunai.

The present invention, as defined by independent claim 1, teaches, among other things, an imager cell including a pinned transfer gate configured to transfer charge between a photoreceptor and a sense node, where a voltage determined by the charge transferred between the photoreceptor and the sense node is read out of the imager cell at the sense node. As disclosed in the present application, a pinned transfer gate is formed from a shallow p++ implanted region in an n-implanted transfer region in a substrate. As disclosed in the present application, the pinned transfer gate is "pinned" because the shallow p++ implanted region is tied (or "pinned") to the potential of the substrate, which is typically at ground or zero volts. As disclosed in the present application, by utilizing a pinned transfer gate to transfer charge between a photoreceptor and a sense node, the present invention advantageously achieves an imager cell that does not require a transistor gate structure, which is conventionally used to transfer charge from the photoreceptor to the sense node.

As disclosed in the present application, photons incident on the photoreceptor produce electrons that are captured in an integration potential well, which is established by an integration voltage V+. As further disclosed in the present application, after the

integration period, a readout potential well is established, which is shallower than the transfer potential established by the pinned transfer gate. As a result, electrons captured by the integration potential well propagate through the transfer potential well into the sense node potential well, where they (i.e. the electrons) can be read. As disclosed in the present application, a source follower can be used to amplify and buffer the resultant potential at the sense node onto a column bus. Thus, by employing a pinned transfer gate situated between a photoreceptor and a sense node, the present invention advantageously achieves the above readout operation without requiring a transistor gate structure.

In contrast, Tsunai does not teach, disclose, or suggest an imager cell including a pinned transfer gate configured to transfer charge between a photoreceptor and a sense node, where a voltage determined by the charge transferred between the photoreceptor and the sense node is read out of the imager cell at the sense node. Tsunai is directed to a solid-state imaging device having an overflow drain, which prevents excessive electrons that cannot be accumulated in a photodiode from overflowing into charge transfer elements or into adjacent pixels and causing undesirable flare and blooming. See, for example, Tsunai, column 3, lines 54-59. Tsunai specifically discloses photodiode N well 16 situated between charge transfer N well 14, which forms charge transfer element 8, and drain 5, which is used to drain off the electrical charge overflowing from photodiode N well 16. See, for example, column 4, lines 13-20 and Figure 2(a) of Tsunai.

Tsunai further discloses a shutter structure, which is achieved by controlling a voltage applied to drain 5 and controlling the width of charge drain control layer 17. See,

for example, column 6, lines 54-60 and Figure 6(a) of Tsunai. In Tsunai, when performing shutter operation and draining away an electrical charge from the photodiode, the voltage applied to the drain causes a short channel effect so that electrons 19 representing signal charge are drained away from photodiode N well 16 into drain 5. See, for example, column 7, lines 17-23 and Figures 6(a) and 6(b) of Tsunai. Thus, in Tsunai, drain 5 is connected to a voltage and used to drain off excessive electrical charge from photodiode N well 16 to prevent flare and blooming. As such, drain 5 is completely different than the sense node recited in independent claim 1, which is used to provide a voltage that can be read out of an imager cell.

On page 5 of the Office Action dated November 3, 2004, the Examiner refers to drain 5 as "sense node 5" and states that "a voltage (note the voltage trace in figure 6b) determined by the charge transferred between the photoreceptor (photodiode 7-16) and the sense node 5 is read out (via readout gate 3) at the sense node 5." However, in Tsunai, readout gate 3 controls the readout of charge from the photodiode while drain 5 is used for the purpose of draining off the electrical charge overflowing from the photodiode. See, for example, Tsunai, column 4, lines 15-20. Thus, drain 5 is not used to provide a voltage that can be read out of an imager cell. As such, drain 5 is not a sense node as recited in independent claim 1. Thus, Tsunai fails to teach, disclose, or suggest an imager cell including a pinned transfer gate configured to transfer charge between a photoreceptor and a sense node, where a voltage determined by the charge transferred

between the photoreceptor and the sense node is read out of the imager cell at the sense node, as recited in independent claim 1.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claim 1, is not suggested, disclosed, or taught by Tsunai. As such, the present invention, as defined by independent claim 1, is patentably distinguishable over Tsunai. Thus claims 5-8 depending from independent claim 1 are, *a fortiori*, also patentably distinguishable over Tsunai for at least the reasons presented above and also for additional limitations contained in each dependent claim.

D. Rejection of Claims 2-34 and 58-71 under 35 USC §103(a)

The Examiner has further rejected claims 2-34 and 58-71 under 35 USC §103(a) as being unpatentable over Tsunai. Independent claims 12, 23, 58, 70, and 71 specify limitations analogous to those specified by independent claim 1. As discussed above, independent claim 1 is patentably distinguishable over Tsunai. Thus, for similar reasons as discussed above, independent claims 12, 23, 58, 70, and 71 are also patentably distinguishable over Tsunai and, as such, corresponding dependent claims 2-11, 13-22, 24-34, and 59-69 are, *a fortiori*, also patentably distinguishable over Tsunai for at least the reasons presented above and also for additional limitations contained in each dependent claim.

E. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1, 12, 23, 58, 70, and 71 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-34 and 58-71 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-34 and 58-71 pending in the present application is respectfully requested.

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Respectfully Submitted,
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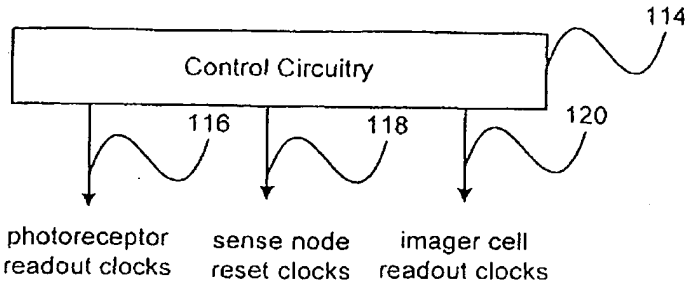
Replacement Sheet



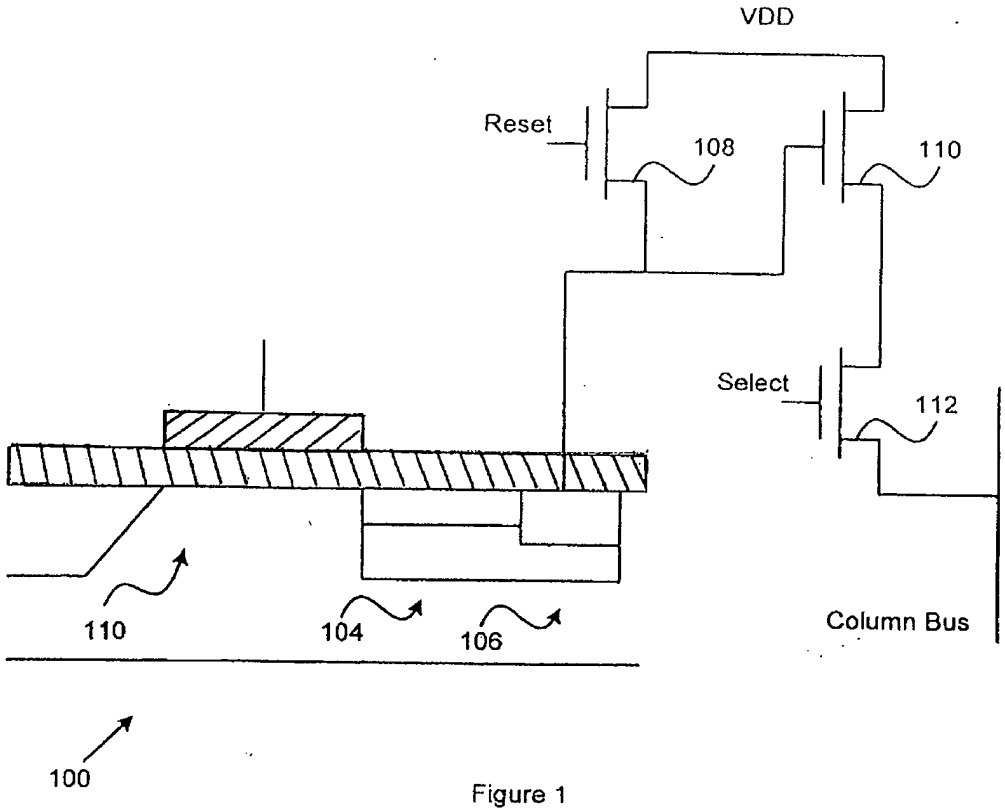


Figure 1

Replacement Sheet

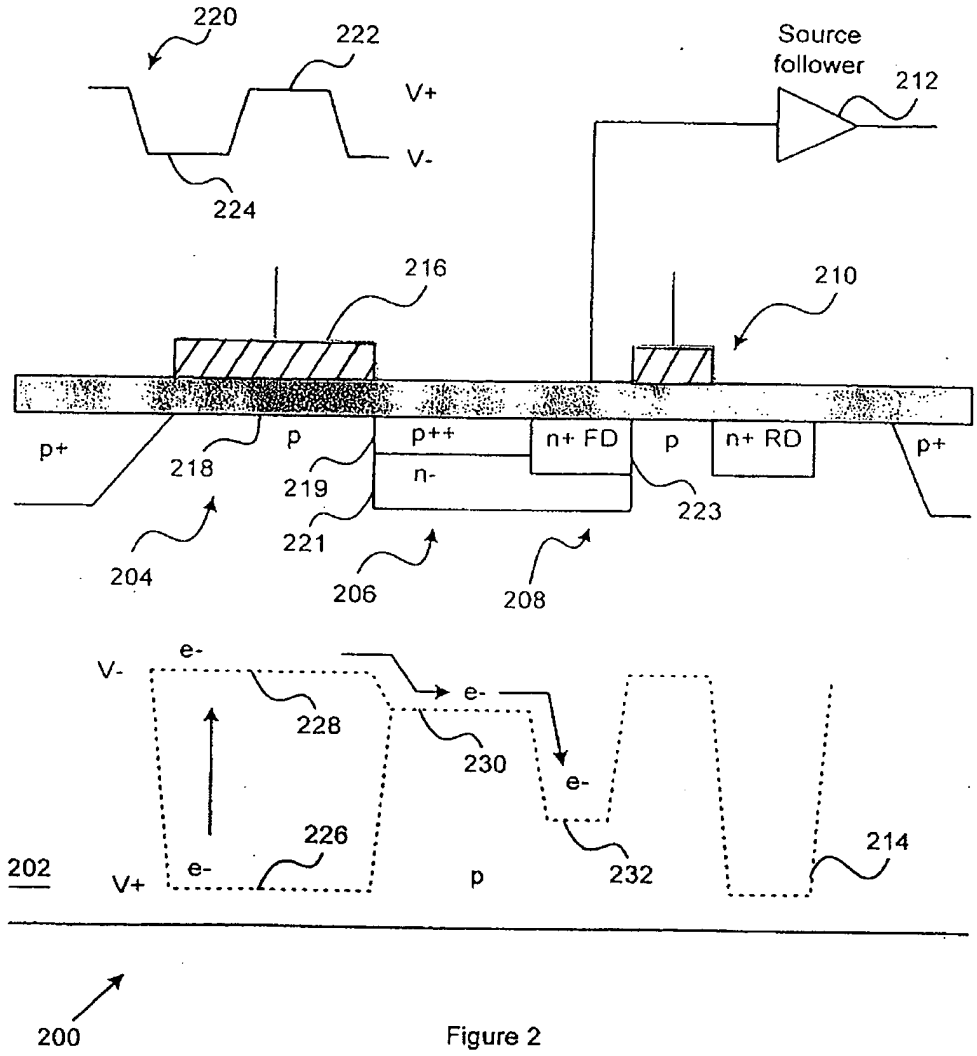


Figure 2

Replacement Sheet

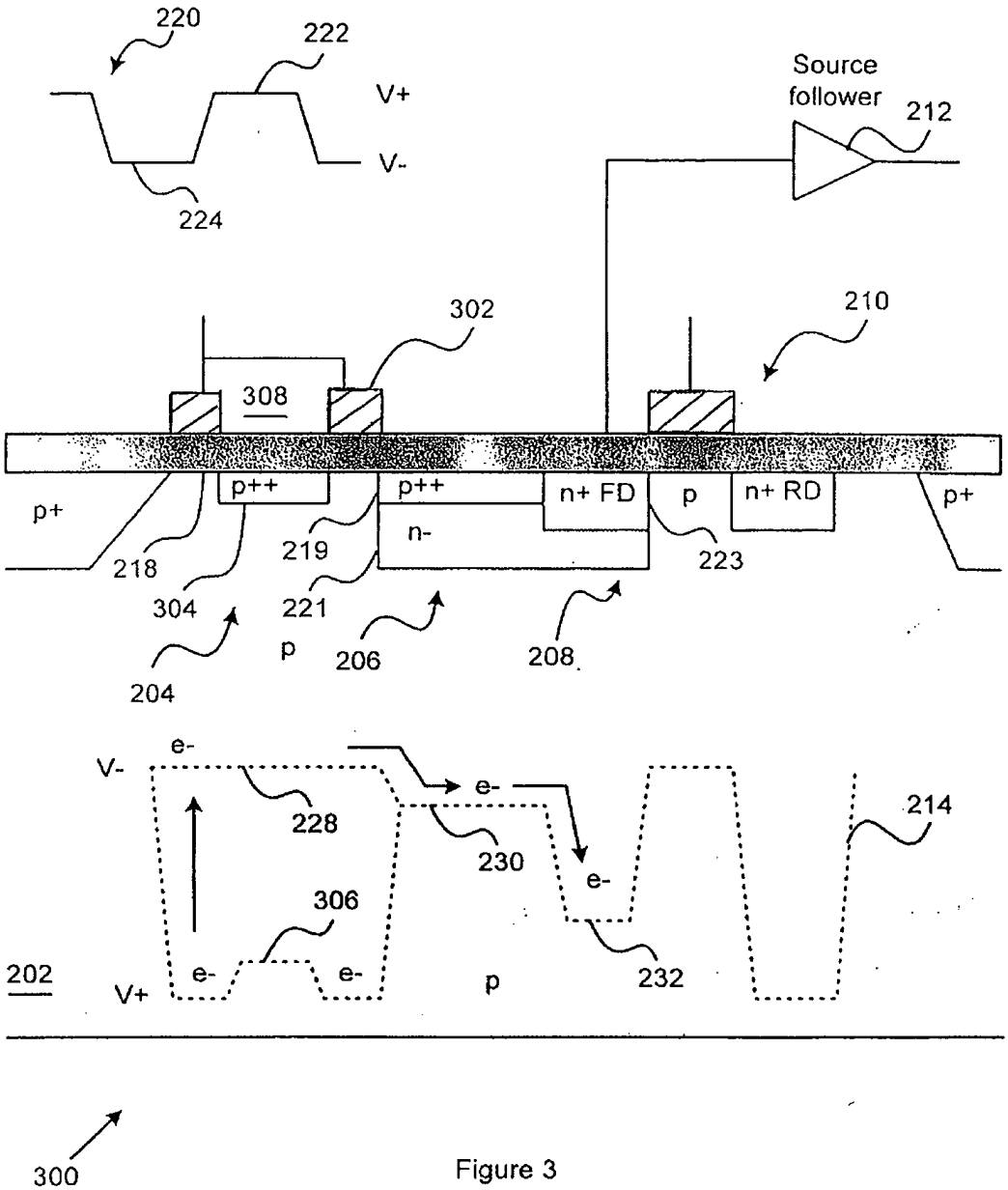


Figure 3

Replacement Sheet

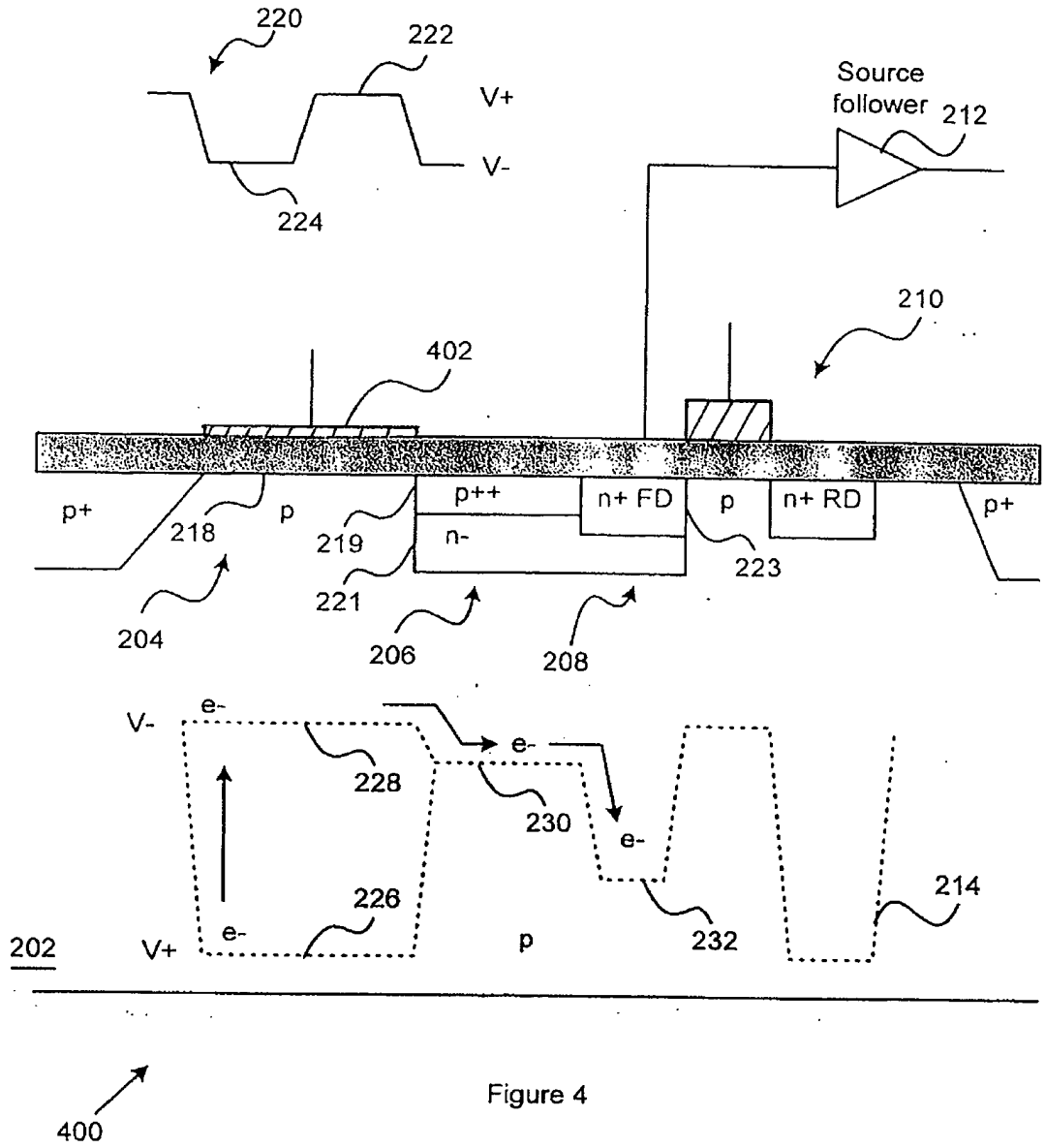


Figure 4

Replacement Sheet

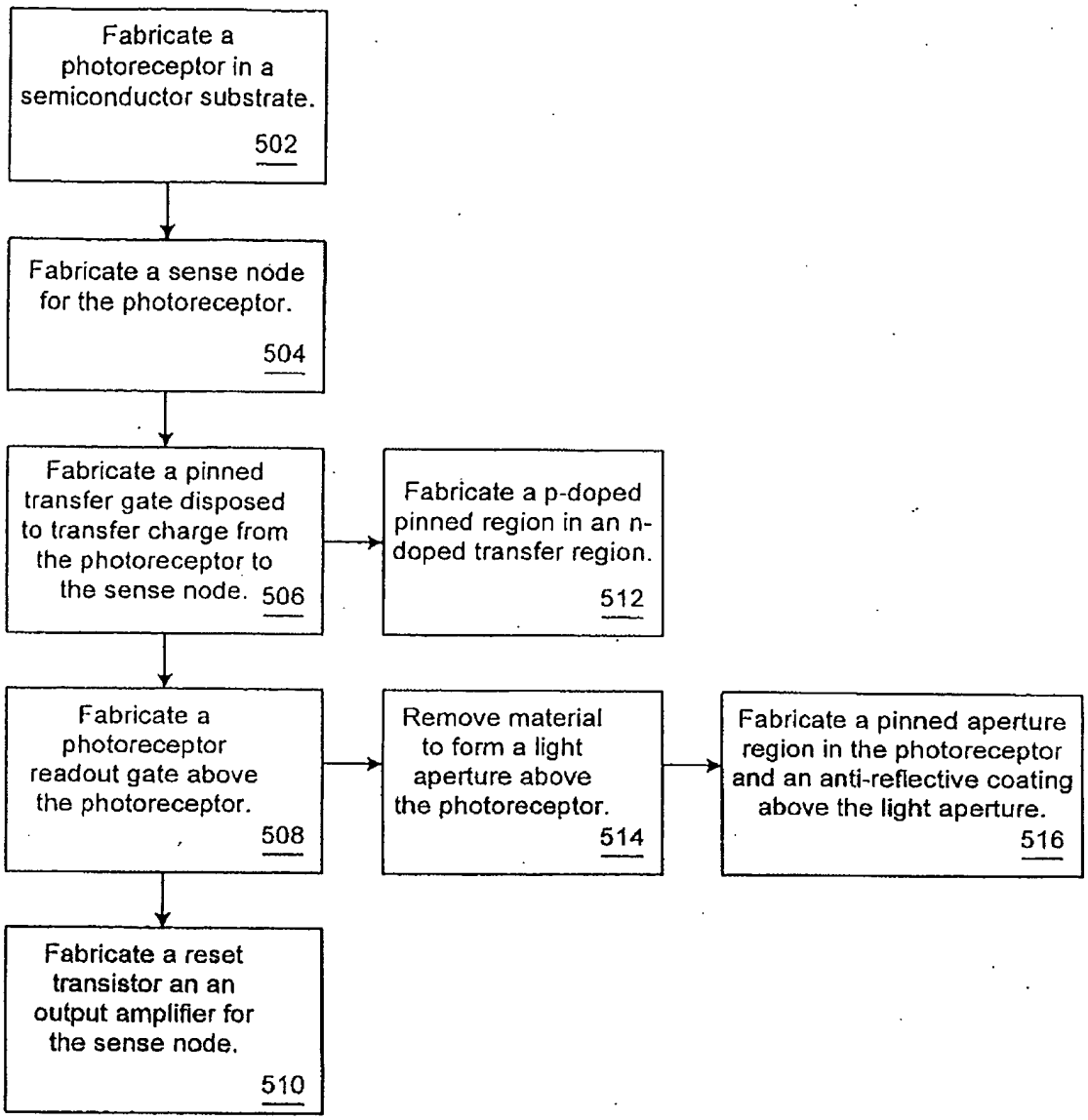


Figure 5

Replacement Sheet

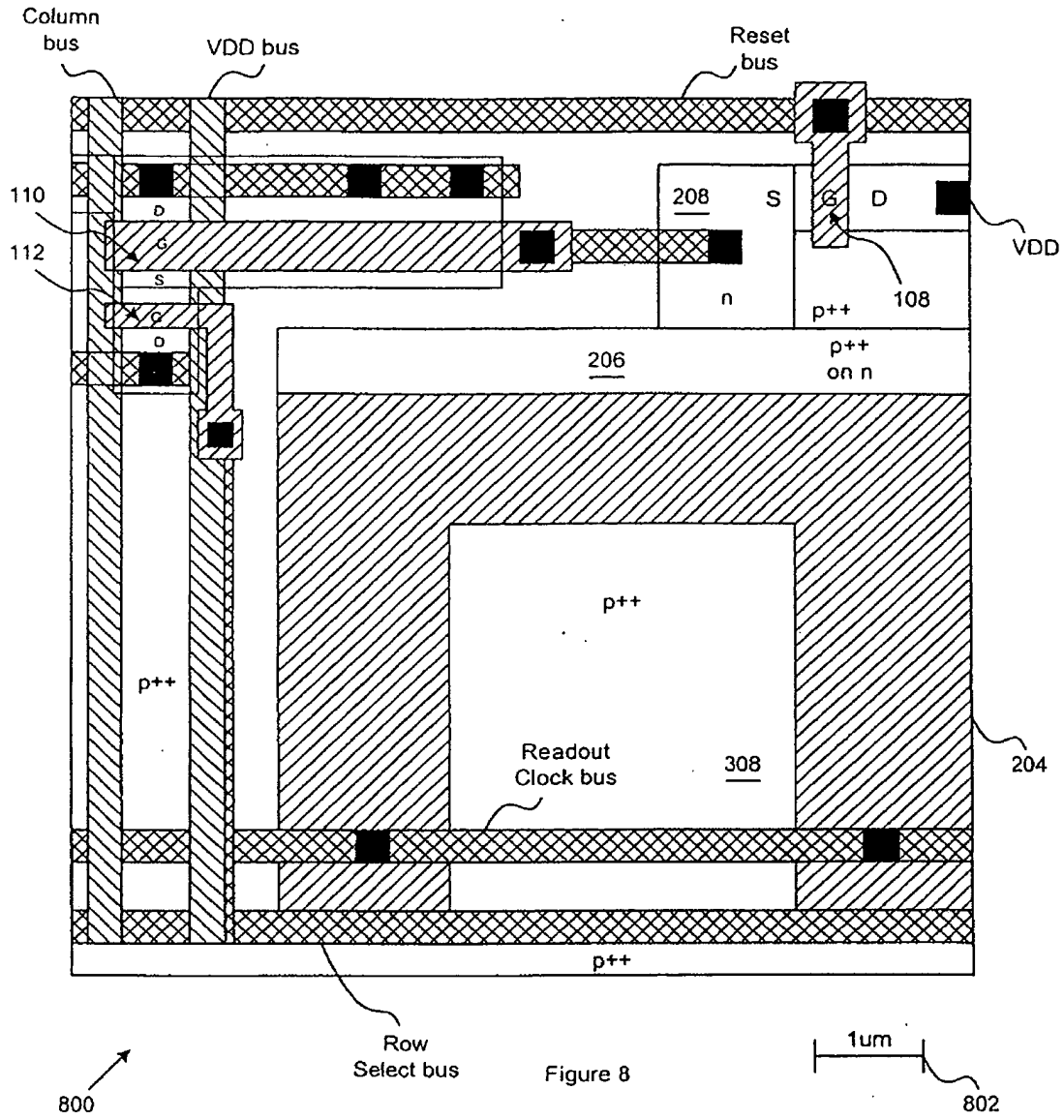


Figure 8